Heterogeneous integration of InAs/GaSb tunnel diode structure on silicon using 200 nm GaAsSb dislocation filtering buffer

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An InAs/GaSb tunnel diode structure was heterogeneously integrated on silicon by solid source molecular beam epitaxy using a 200 nm strained $GaAs_{1-y}Sb_y$ dislocation filtering buffer. X-ray analysis demonstrated near complete strain relaxation of the metamorphic buffer and a quasi-lattice-matched InAs/GaSb heterostructure, while high-resolution transmission electron microscopy revealed sharp, atomically abrupt heterointerfaces between the GaSb and InAs epilayers. In-plane magnetotransport analysis revealed Shubnikov-de Haas oscillations, indicating the presence of a dominant high mobility carrier, thereby testifying to the quality of the heterostructure and interfaces. Temperature-dependent current-voltage characteristics of fabricated InAs/GaSb tunnel diodes demonstrated Shockley-Read-Hall generation-recombination at low bias and band-to-band tunneling transport at high bias. The extracted conductance slope from the fabricated tunnel diodes increased with increasing temperature due to thermal emission (E_a ~ 0.48 eV) and trap-assisted tunneling. Thus, this work illustrates the significance of defect control in the heterointegration of metamorphic InAs/GaSb tunnel diode heterostructures on silicon when using $GaAs_{1-y}Sb_y$ dislocation filtering buffers.
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I. INTRODUCTION

Tunneling field-effect transistors (TFETs) have been extensively studied[1–20] for their application to low-power digital logic due to their (i) steep subthreshold-swing (*SS*) characteristics, (ii) high drive current (I_{ON}), (iii) low threshold voltage (V_{TH}), and (iv) high ON-state to OFF-state current ratio (I_{ON}/I_{OFF}). One enticing approach towards the realization of TFET devices is the adoption of heterogeneous material systems (*e.g.*, $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$), thereby allowing device designers to tailor the effective tunneling barrier height (E_{beff}) *via* alloy composition.[11,12,21–23] Although mixed arsenide/antimonide-based TFET architectures have shown progress in realizing step *SS* (<60 mV/dec)[10,20] and low E_{beff} (<0.5 V) operation, they have been limited to smaller diameter, cost-prohibitive III-V substrates. Therefore, the heterogeneous integration of a mixed As/Sb material system (*e.g.*, broken-gap InAs/GaSb) on Si would be a significant step towards the integration of III-V TFETs into the Si CMOS process flow. However, the heterogeneous integration of mixed As/Sb device structures faces several challenges due to differences in material properties, including:

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(i) thermal expansion coefficient mismatch-induced stress;[24] (ii) anti-phase domain formation due to polar (III-V) on non-polar (Si) heteroepitaxy; and (iii) lattice mismatch-induced crystal defects and dislocations.[25–28]

Several approaches have been implemented to address these challenges, such as metamorphic buffer architectures,[25–32] strained-layer superlattice buffers,[25,33] migration enhanced epitaxy utilizing off-cut substrates,[34–38] combined low- and high-temperature growth phases interspersed with thermal cycling annealing,[39–48] and the intentional formation of interfacial misfit dislocation (IMF) arrays at the substrate/buffer heterointerface.[49,50] Specific to InAs/GaSb-based tunnel FET structures on Si, Bhatnagar *et al.*[51] employed off-cut Si substrates along with (i) a combined IMF/III-Sb metamorphic buffer, and (ii) an *in-vacuo* $SrTiO_3$ and III-As buffer also utilizing IMF array formation. The large defect density present in the metamorphic TFET structures on Si, grown *via* the oxide or semiconductor buffer approach, resulted in deteriorated device performance as compared to control devices demonstrated on GaSb. Thus, the results of Bhatnagar *et al.*[51] indicate that a metamorphic buffer architecture must have a matching growth process capable of producing low defect densities in order to successfully integrate mixed As/Sb TFETs on Si. In order to demonstrate the feasibility of such a heterogeneous integration scheme, we comprehensively investigate the design, material synthesis and analysis, magnetotransport characteristics, and electrical properties of as-grown and fabricated InAs/GaSb tunnel diode heterostructure heterogeneously integrated on Si using a 200 nm strained $GaAs_{1-y}Sb_y$ dislocation filtering buffer. The proposed metamorphic buffer architecture addresses the tandem issues of defect propagation (into the active layers) and a reduction in buffer thickness, thus enabling cost-effective III-V/Si heterointegration. Moreover, careful As and Sb shutter sequencing was implemented, resulting in a minimization of atomic intermixing and segregation through precise atomic flux control[21,42] and thereby reducing interfacial roughness, disorder, and defects. Leveraging this methodology, we successfully demonstrate the integration of InAs/GaSb tunnel diode heterostructures on Si using molecular beam epitaxy (MBE).

II. EXPERIMENTAL

The InAs/GaSb tunnel diode heterostructure shown in Figure 1 was grown using solid-source MBE on a (100)Si substrate offcut 4° toward the <110> direction. A composite GaAs/200 nm strained $GaAs_{1-y}Sb_y$/GaAs/GaSb buffer scheme was used to promote efficient film relaxation and minimize dislocations while also minimizing total buffer thickness. The incorporation of a strained $GaAs_{1-y}Sb_y$ layer provided additional strain energy during buffer growth, enhancing dislocation glide for threading dislocations (TDs) propagating into the $GaAs_{1-y}Sb_y$ epilayer and minimizing further TD propagation upward into the active layer. The Si substrate was pre-cleaned using a modified RCA process in which the native oxide removal was performed last, *i.e.*, immediately prior to loading of the sample into the MBE growth system. Following a 120 min, 180°C load-lock bake, the Si substrate was immediately transferred to the III-V growth chamber for subsequent oxide desorption at 950°C. Upon achieving an oxide-free Si surface, as monitored by *in-situ* reflection high-energy

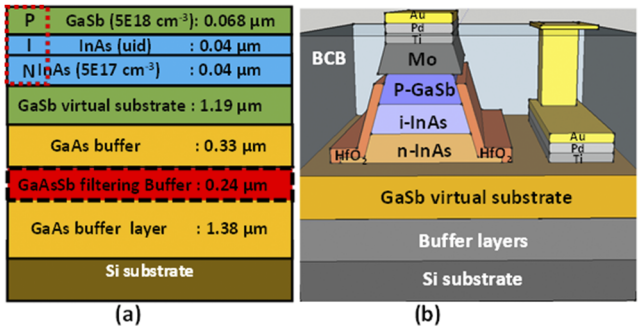

FIG. 1. Cross-sectional schematics of (a) as-grown InAs/GaSb material stack and (b) fabricated InAs/GaSb *p-i-n* tunnel diode integrated on to Si.

electron diffraction (RHEED), the substrate temperature was lowered to 375°C for low-temperature GaAs nucleation. We note that the temperatures referred to herein are the thermocouple temperatures. A standard two-step growth process[46,47,52] was used for the initial GaAs buffer prior to growth of the subsequent strained $GaAs_{1-y}Sb_y$ dislocation filtering epilayer. Additionally, a five-step thermal cycle annealing (TCA) scheme was incorporated into the GaAs buffer growth in order to enhance dislocation glide and annihilation. The low growth temperature ≤ 425°C (measured by thermocouple), low growth rate (~0.1μm/hr, measured by reflection high energy electron diffraction) and As/Ga fluxes ratio of ~12 were used during the 300Å thickness of GaAs nucleation layer growth using migration enhanced epitaxy (repetition of As and Ga fluxes) after the thermal desorption of oxides from Si surface. As the TCA was needed to minimize TDs for subsequent GaAs layer growth, 5-steps TCA annealing schemes (1-step: 400°C-425°C→650°C→400°C-425°C) were implemented inside the GaAs layer prior to GaAsSb dislocation filtering buffer layer growth. The remainder of the growth was periodically monitored *via* RHEED, excluding the critical InAs/GaSb heterointerface. Si and beryllium (Be) were used as dopants for *n*-type InAs and *p*-type GaSb, respectively. Detailed growth parameters, such as growth rates, flux ratios, and growth temperatures for InAs and GaSb, respectively, can be found in Ref. 21.

In order to validate the successful heterointegration of III-V active device layers on Si using the proposed buffer architecture, we have characterized the structural properties of the as-grown heterostructure, including the: (i) strain-state *via* x-ray diffraction; (ii) defect density *via* transmission electron microscopy (TEM); and (iii), surface morphology *via* atomic force microscopy (AFM). The defect density inside the GaAs and the active device layer were approximately $5x10^8$-$1x10^9$ cm^{-2} and $1x10^7$ cm^{-2}, respectively. The strain relaxation properties of the InAs/GaSb heterojunction tunnel diode grown on Si were determined by high-resolution x-ray diffraction using a PANalytical X'pert Pro system equipped with a Cu $K\alpha_1$ x-ray source. Both symmetric (004) and asymmetric (115) reciprocal space maps (RSMs) from the InAs/GaSb heterostructure on Si were obtained in order to determine the relaxation state of the GaAs and $GaAs_{1-y}Sb_y$ buffers and the crystal quality of the InAs and GaSb epilayers. Additionally, the defect properties of the complete multi-layer structure, along with the material and interface quality of the InAs/GaSb active region, were evaluated using high-resolution TEM analysis using a JEOL 2100 TEM. TEM samples were prepared by mechanical polishing, dimpling, and low-temperature (-120°C) Ar^+ ion-milling. In-plane magnetotransport measurements were performed using a van der Pauw geometry at low temperatures and in magnetic fields B up to ± 9 Tesla. A ^{3}He cryostat with the sample submerged in liquid ^{3}He was utilized in order to obtain cryogenic sample temperatures. The sample current was then applied in the plane of the layers, whereas B was applied normally to the plane of the layers. Lastly, tunnel diodes were fabricated from using a previously described[53,54] vertical heterojunction tunnel FET fabrication process flow. In brief, a sputter-deposited 300 nm molybdenum (Mo) contact/etch mask was deposited on the top-most GaSb epilayer. The etch mask for the diode mesa was then defined using electron-beam lithography (EBL) followed by a 30 nm Ti/60 nm Cr electron-beam (e-beam) evaporation and metal lift-off process. An inductively coupled plasma dry etch process using a chlorine (Cl_2)-based etchant was used to etch the diode mesa until the GaSb/InAs tunnel-junction was exposed, whereas the mesa sidewalls were passivated using 4 nm atomic layer deposited HfO_2. The n^+-InAs (source) contact was patterned using EBL on the bottom-most InAs layer followed by e-beam evaporation of 20 nm Ti/20 nm Pd/30 nm Au contact metals. The Mo/p^+-GaSb (drain) contact (20 nm Ti/20 nm Pd/60 nm Au) was formed using e-beam evaporation and an EBL process on top of the mesa structure. Benzo chlorobutane (BCB) was used as an inter-level dielectric, which was finally etched back to access the source contact pad for measurement. Diode electrical properties were evaluated using an ARS Cryo-made temperature-dependent, ultra-high vacuum probe station (in the temperature range of 77 K to 290 K) interfaced with a Keithley 4200-SCS semiconductor parameter analyzer.

III. RESULTS AND DISCUSSIONS

A. Strain relaxation properties

Figures 2, 3, and 4 show the x-ray rocking curve, (004) symmetric and (115) asymmetric reciprocal space maps, respectively, of the InAs/GaSb tunnel diode structure on Si, the structure of which

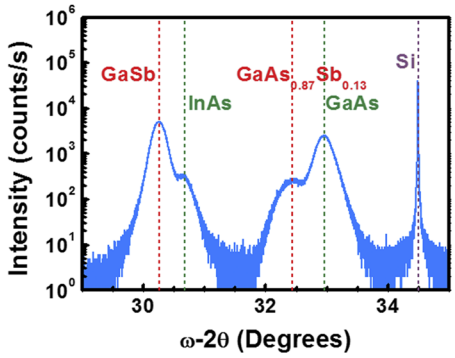

FIG. 2. High-resolution x-ray rocking curve from the (004) Bragg line of InAs/GaSb tunnel FET structure grown on Si substrate using metamorphic and GaAsSb dislocation filtering buffer architecture.

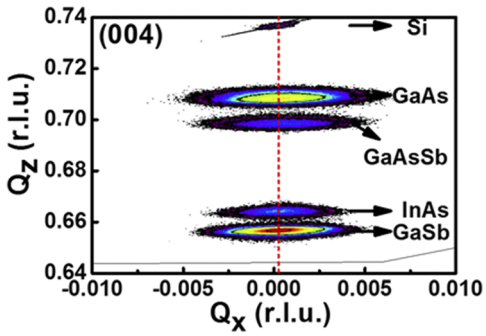

FIG. 3. (004) RSM of the as-grown heterostructure. All RLPs are aligned with respect to Q_Z, indicating minimal lattice tilt.

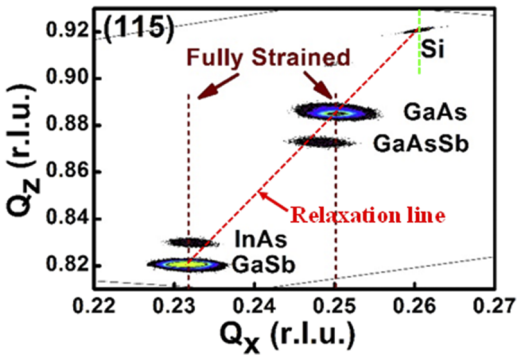

FIG. 4. (115) RSM of the as-grown heterostructure. The InAs and GaSb RLPs are vertically aligned in Q_Z, indicating fully strained InAs epitaxy. The $GaAs_{0.87}Sb_{0.13}$ epilayer shows partial relaxation, and was used as a dislocation filter.

is shown in Fig. 1. The reciprocal lattice point (RLP) of the strained $GaAs_{1-y}Sb_y$ dislocation filtering buffer can be found slightly below (in Q_z) that of the GaAs metamorphic buffer. The broadening of both the GaAs and GaSb RLPS, when compared to the Si substrate, can be attributed to lattice mismatch-induced defects and dislocations generated *via* strain relaxation during growth. From Figs. 3 and 4, one can determine the out-of-plane and in-plane lattice constants, respectively, of each epilayer and hence their associated strain relaxation properties. The GaAs and GaSb epilayers were found to be fully relaxed with respect to the Si substrate, as expected for the growth techniques employed in this work. In addition, one can find from Fig. 4 that the RLP of the strained $GaAs_{0.87}Sb_{0.13}$ epilayer lies between the relaxation and strain vectors of the Si substrate and GaAs epilayer, respectively, indicating a partial relaxation of the in-grown $GaAs_{0.87}Sb_{0.13}$ strain. On the other hand, the

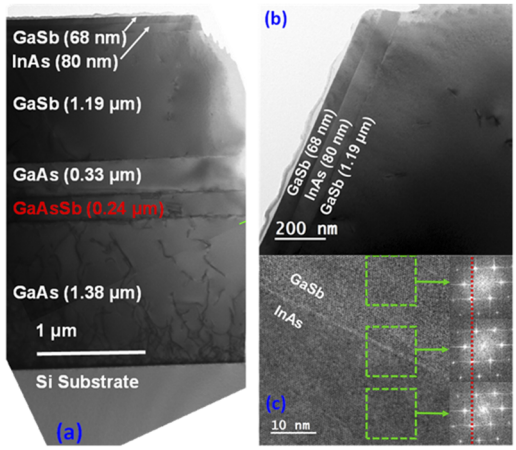

FIG. 5. (a) Cross-sectional TEM micrograph of the entire heterostructure. The $GaAs_{0.87}Sb_{0.13}$ layer prevents TDs from propagating into the InAs/GaSb active region; (b) Cross-sectional TEM micrograph of the active device region; and (c) HRTEM and fast Fourier transforms (FFTs) of the tunneling interface. The FFTs further confirmed that InAs is fully strained with respect to GaSb.

InAs and GaSb RLPs were found to be vertically aligned in Q_Z, indicating a fully strained heterointerface absent of quantifiable relaxation within the sensitivity limits of the diffractometer. Additionally, one can find from the vertical alignment of RLPs in Fig. 3 that no significant lattice tilt was generated during the relaxation of the metamorphic buffer(s), *i.e.*, the GaAs, $GaAs_{0.87}Sb_{0.13}$, and GaSb epilayers. The strain relaxation properties and the strain dislocation filtering buffer layer were further evaluated by analyzing cross-sectional TEM micrographs of the heterostructure.

B. Heterointerface analysis

Figure 5(a)–(c) shows the cross-sectional TEM micrographs of the entire tunnel diode heterostructure including the (a) GaAs/$GaAs_{0.87}Sb_{0.13}$/GaAs strained-layer metamorphic buffer on Si, (b) InAs/GaSb active region, and (c), Fast Fourier Transform (FFT) patterns taken across the InAs/GaSb heterointerface, respectively. The thickness of each layer and its associated material have been labeled in Fig. 5, wherein one can correlate the structure shown in Fig. 1 with the labeled epilayers identified in Fig. 5(a). Dislocations due to lattice mismatch and associated strain relaxation were predominately confined within the initial ~1.4 μm GaAs buffer. The $GaAs_{0.87}Sb_{0.13}$ dislocation filtering buffer was effective at limiting TD propagation upward through the remaining epilayers, as evidence by the strong strain-field contrast at the GaAs/$GaAs_{0.87}Sb_{0.13}$/GaAs heterointerfaces and the significantly enhanced TD glide observed particularly at the bottom GaAs/$GaAs_{0.87}Sb_{0.13}$ interface. In addition, the GaSb virtual substrate was observed to relax primarily *via* the formation of an interfacial misfit array at the GaSb/GaAs interface (shown in Fig. 6), as evidenced by the minimal presence of crystal defects throughout the GaSb epilayer, in agreement with previously reported work.[42,49,50]

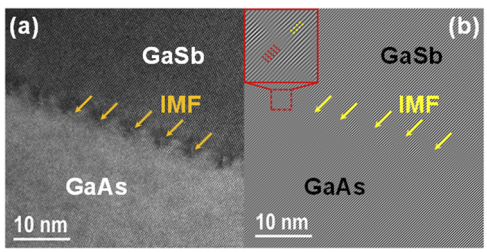

FIG. 6. (a) High-resolution micrograph of GaSb/GaAs heterointerface showing the interface misfit dislocations and (b) filtered FFT pattern of the same GaSb/GaAs heterointerface showing Lomer dislocations (yellow arrow) periodically separated, corresponding to a near-complete GaSb buffer relaxation.

We can conservatively estimate the threading dislocation density in the active layer at approximately 10^7 cm^{-2}.[55] Moreover, the FFT patterns show an absence of diffraction spot splitting or of satellite peaks from the InAs-GaSb heterointerface, indicating a coherent interface and quasi-ideal InAs/GaSb strained heteroepitaxy, in agreement with our x-ray results presented above (*see* Figure 4). The confinement of defects and dislocations within the GaAs metamorphic buffer, further reduced by the addition of a strained $GaAs_{0.87}Sb_{0.13}$ dislocation filtering buffer, is expected to improve the carrier transport properties of this structure.

C. Surface morphology

Figure 7 shows a representative AFM micrograph of a 20 μm × 20 μm region taken from the top surface of the tunnel diode structure. One can find from this figure that the top p^{++}-GaSb surface exhibited low root-mean-square (*rms*) roughness and high uniformity over the measured region. An *rms* roughness of 3.7 nm was found to be consistent to that of heteroepitaxially-grown MBE $In_{0.7}Ga_{0.3}As$ films or lattice-mismatched III-V semiconductors on Si ($4\% < f < 8\%$) utilizing metamorphic graded buffers.[12,19,46,47,56] The low measured *rms* roughness is also consistent with RHEED observations during growth, which displayed an elongated (1×3) surface reconstruction pattern for the GaSb source, thereby indicating a highly uniform arrangement of the top-most atomic layer. The improved surface morphology of the InAs/GaSb film on Si is comparable to lattice mismatched epitaxy reported in the literature[12,19,46,47,51] is due to the fine control over III-V nucleation and TD glide dynamics through the combined GaAs growth optimization and strained $GaAs_{0.87}Sb_{0.13}$ dislocation filtering buffer.

D. Magnetotransport properties

To further investigate the material quality of the InAs/GaSb tunnel diode heterostructure grown on Si, low-temperature in-plane magnetotransport experiments were performed (sample current in the plane of the layers, B normal to the plane of the layers). Although the *p-i-n* tunnel diode would nominally operate *via* vertical transport (sample current normal to the plane of the layers), in-plane transport can reveal if in-plane disorder is present due to, among other causes, interdiffusion, interface roughness, residual impurities, dislocations, *etc.*, in the active *p-i-n* layers. Figure 8 shows the in-plane longitudinal transport coefficient (measured potential gradient parallel to applied current), R_{XX}, symmetrized in B, plotted as magnetoresistance *vs.* B at a temperature of 390 mK. In Fig. 8, Shubnikov-de Haas oscillations are apparent, testifying to the existence of carriers with high in-plane mobility (μ), resulting from the superior interface uniformity and abruptness. It is worth noting that

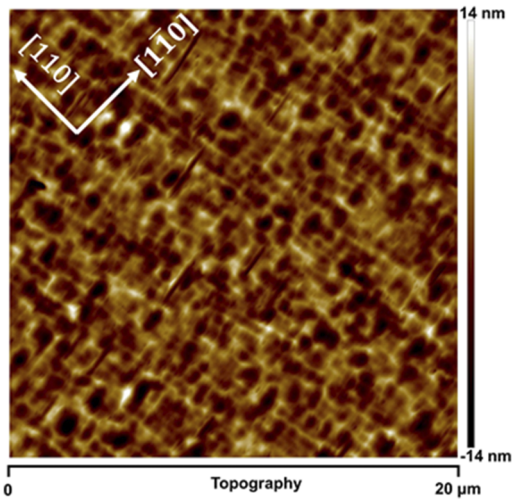

FIG. 7. AFM micrograph of the GaSb/InAs surface of the as-grown tunnel diode heterostructure. A low *rms* roughness of 3.7 nm was observed.

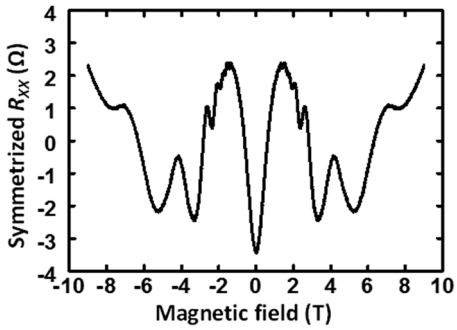

FIG. 8. In-plane longitudinal transport coefficient R_{XX}, symmetrized in magnetic field, plotted as magnetoresistance *vs.* magnetic field at a temperature of 390 mK.

Shubnikov-de Haas quantum oscillations typically appear at low temperatures in materials with low disorder, where both thermal and disorder-induced Landau level broadening are minimal.[57] Disorder-induced Landau-level broadening can be expressed in a minimal product μB, implying that the carrier population in the active *p-i-n* InAs and GaSb layers possesses a high μ and hence a long momentum transport relaxation time. The high carrier μ in the InAs/GaSb heterostructure on Si is likely promoted by the low dislocation density in the active *p-i-n* layers. From the Shubnikov-de Haas oscillations, the areal density of the carrier population responsible for the oscillations can be obtained. At low B, a single frequency from a single carrier type was observed, while at higher B the oscillations were more complex. This could indicate that at higher μB, another lower-μ carrier also contributes to conduction. From Fig. 8 the carrier density corresponding to the observed low-B Shubnikov-de Haas oscillations was found to be $N_s = 4.34 \times 10^{15}\, m^{-2}$ at 390 mK. This areal density cannot be directly related to the low-temperature value of carrier densities in the InAs or GaSb layers, because the in-plane transport cannot from the present experiments distinguish contributions from carriers in the respective InAs and GaSb layers. The order of magnitude for the measured low-temperature N_s is however compatible with the InAs and GaSb bulk doping levels and *p-i-n* layer thicknesses in Fig. 1(a).

E. Electrical transport characteristics of InAs/GaSb tunnel diode

Figure 9 shows a tilted-view scanning electron micrograph (SEM) micrograph of a fabricated InAs/GaSb tunnel diode. Figure 10 shows the current density-voltage (J-V) characteristics from a representative InAs/GaSb tunnel diode on Si measured at different temperatures, ranging from 79 K to 300K. One can find from Fig. 10 that under forward bias, the J-V characteristics exhibited a strong dependence on temperature. The negative differential resistance (NDR) effect is not visible on these diodes and it was believed due to sidewall interface traps present at III-V and high-κ interface,[58] one of the major limiting factors for tunnel diodes and transistors. These diodes are most likely suffering parasitic conduction from surface states which is masking the NDR effect. An Arrhenius plot presented in Figure 11 depicts the current density of the device as an inverse function

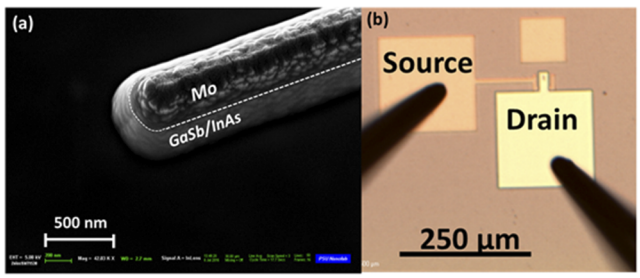

FIG. 9. (a) Tilted-view SEM micrograph of a fabricated tunnel diode. The area of the fabricated diode is 0.875 μm^2. (b) Optical image of a fabricated InAs/GaSb *p-i-n* tunnel diode showing the source (InAs) and drain (GaSb) contact pads.

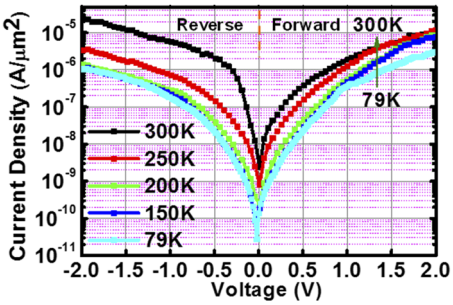

FIG. 10. Temperature-dependent J-V characteristics. The forward bias behavior shows a strong temperature dependence due to the presence of significant thermal emission current.

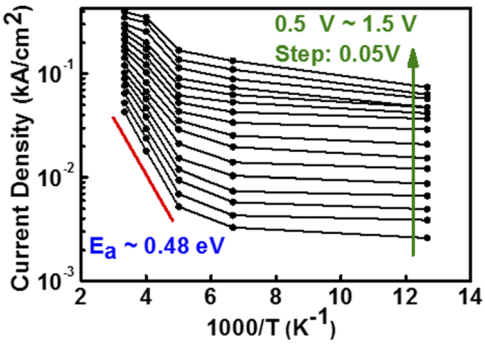

FIG. 11. Temperature dependence of diode current density as a function of inverse temperature with various applied voltages. The two different slope regions indicate different current generation mechanisms.

of measurement temperature with varying voltage (0.5 V to 1.0 V) under forward bias. Fig. 11 can be further differentiated into two regions: (i) a steep slope region, and (ii) a shallow slope region. The low temperature region of Fig. 11, *i.e.*, the shallow slope region, can be attributed to tunneling current in the absence of additional current generation mechanisms, that is, when all other carriers freeze out. At higher temperatures, *i.e.*, within the steep slope region, the slope $(\log(J)/(1000/T)$ represents an activation energy (E_a) and gradually decreases with increasing bias. The extracted activation energy ($E_a \sim 0.48$ eV) at 0.5 V is similar to the valence band barrier for hole thermal emission from the GaSb valence band edge to the InAs valence band edge, which is the sum of the InAs bandgap (0.35 eV) and the valence and offset (0.18 eV), as depicted in Figure 12. One can infer that the barrier for holes is approximately triangular in shape, which can result in hole tunneling

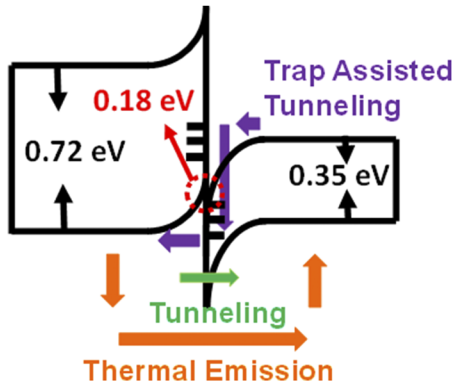

FIG. 12. Schematic band diagram under forward bias highlighting the different current generation mechanisms and carrier paths.

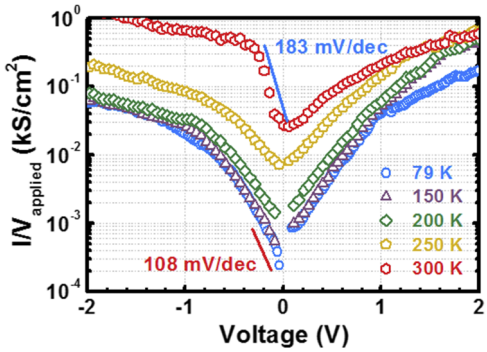

FIG. 13. Conductance–voltage relationship as a function of temperature. The reverse bias region can be used to predict the subthreshold slope of a TFET device.

without thermal excitation. The effect of increasing bias voltage is to enhance the tunneling probability by reducing the barrier width such that holes can tunnel at lower energy. As a result, the effective activation energy decreases with increasing bias, which is consistent with the measured data shown in Fig. 11.

The conductance slope method can give an approximate prediction of the subthreshold slope (*SS*) of a three-terminal TFET by using a two-terminal tunnel diode.[59] Moreover, this method can be used to evaluate the impact of tunnel junction interface properties on the predicted *SS* of a TFET device. The temperature-dependent conductance slope is extracted from an (I/V_a)-V_a plot, as shown in Figure 13. The slope is expressed in mV/decade and is located in the reverse bias region, that is, in the same operating regime as a TFET with a positive applied voltage. With increasing temperature, the conductance slope also increases due to the thermal enhancement of leakage mechanisms, such as thermal emission and trap-assisted tunneling. There might be some leakage paths contributing from both small pits and the electrically active oxide trap on the side wall of the mesa. Unfortunately, it is difficult to distinguish the possible contribution of each from the measured current. Further experimental and theoretical work are necessary to quantify the side wall current of mesa for tunnel diode. Lastly, Figure 14 presents a benchmark of the results from this work along with previously published data for InAs/GaSb, InAs/$GaAs_{1-y}Sb_y$, $In_xGa_{1-x}As$/InAs, GaSb/InAsSb, and $In_xGa_{1-x}As$/InP-based material systems, all of which were grown on lattice-matched III-V substrates.[60–66] All TFET devices show stronger temperature dependence than two terminal devices, indicating that thermal processes are dominant in these devices and that interface engineering will play a key role in realizing mixed As/Sb TFETs on Si with *SS* approaching the thermal limit.

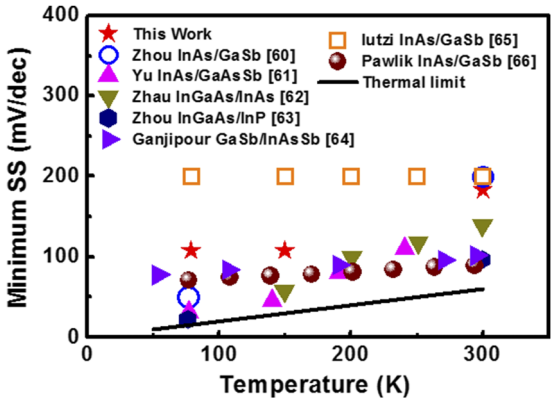

FIG. 14. Benchmarking of the minimum conductance slope as a function of temperature. This work provides comparable predicted subthreshold slope to that of other As-Sb-based tunnel diode/TFET heterostructures.

IV. CONCLUSIONS

An InAs/GaSb tunnel diode heterostructure was grown on Si by solid-source molecular beam epitaxy. The structural, morphological, heterointerface, and magnetotransport characteristics of the InAs/GaSb heterostructure were investigated by high-resolution x-ray analysis, transmission electron microscopy, and magnetotransport measurements as a function of magnetic field. High-resolution TEM analysis revealed atomically-abrupt transitions between the GaSb and InAs active layers. Magnetotransport analysis revealed Shubnikov-de Haas oscillations, testifying to the high material quality of the heterostructure and heterointerfaces. Current-voltage characteristics, measured as a function of temperature, of fabricated InAs/GaSb *p-i-n* tunnel diodes demonstrated Shockley-Read-Hall generation-recombination at low bias and band-to-band tunneling transport at high bias. With increasing temperature, the extracted conductance slope also increased due to enhanced leakage, mirroring tunnel diode behavior on III-V substrates. An activation energy of 0.48 eV was found, correlating to thermal emission from the GaSb valence band edge to the InAs valence band edge. These results elucidated the importance of defect control in metamorphic InAs/GaSb tunnel diode heterostructures on Si. Further optimization of the $GaAs_{1-y}Sb_y$ strained-layer/buffer processes will pave the way for future multifunctional device co-integration on Si.

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