**Designing Data Read Out Electronics for the CHANDLER Neutrino Detector**

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**Introduction**

CHANDLER (Carbon Hydrogen ANtineutrino Detector with a Lithium Enhanced Raghavan optical lattice) is a reactor neutrino detector technology. The CHANDLER technology consists of layers of wavelength shifting plastic scintillator cubes separated by thin sheets of lithium-6 loaded zinc sulfide. In inverse beta decay, when an electron antineutrino scatters off a proton, it creates a positron and a neutron. Lithium-6 is used to capture the neutron. The light that is produced by the scintillator cubes is then guided to the PMTs by total internal reflection.

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**Old Electronics**

The old electronics for MiniCHANDLER consisted of shapers and CAEN digitizers with a 12-bit ADC. The 12-bit ADC was not able to effectively measure higher energy neutron proton recoils, because it exceeds the range. Another problem with the old electronics was that there was cross-talk between neighboring channels, due to the single-ended input of the PMT signal. Moreover, the trigger algorithm would fail under high energy pulses, because it would cause large oscillations in the baseline. These oscillations caused retriggers and at times the inability to read low pulse height neutron signals. If the trigger threshold was set to a normal level the digitizer would send too much information, using too much bandwidth. To compensate for this the trigger threshold was raised, which led to missing vital information.

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**New Electronics**

The development of the new electronics is geared toward improving the old electronics. The new electronics will have no crosstalk, better dynamic range, no oscillating after effects, take up less space, and be cheaper. One addition to the new electronics that improves flexibility is the FPGA. The FPGA allows for more complex codes to be used, which can be used to fix some of the previous problems. One problem that is going to be improved because of the FPGA is the trigger algorithm which has the running baseline code.

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**Read Out Firmware**

The FPGA uses VHDL as the coding firmware. The running baseline code characterizes the baseline allowing the pretrigger window to be analyzed. The running baseline will send out the sum of the ADC counts, moving average, ADC values squared, sum of ADC squared, and moving average squared. These all could be used as important indicators to compensate for the running baseline not being perfectly flat. Two pretrigger windows are expected. These are a relatively flat baseline and exponential decay.

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**Sources**

